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| | **US ATLAS<br>PHASE I Upgrade<br>BASIS of ESTIMATE (BoE)** | **Date of Est: 5/2/14<br>Rev 8/26/14**<br>**Prepared by: Gustaaf Brooijmans<br>Responsible Inst: Columbia U.**<br>**Docdb #:** |
| **WBS number: 1.1.3.2.1** | **WBS Title: ASIC ADC for LTDB** | |
| **WBS Dictionary Definition:**<br>Analog signals on the LTDB need to be digitized at 40 MHz before transmission off-detector. This WBS covers the development and production of an ASIC ADC fulfilling the requirements for the LTDB: digitize at 40 MSPS, 12-bit dynamic range with 11-bit precision, low power (< 150mW/channel), low latency (as low as possible, certainly < 200 ns), radiation tolerant (HL-LHC requirements), small form factor with serialized outputs. The cost includes design, prototyping, production, packaging, testing and assistance in integration. About 10,000 4-channel ADC chips will be needed. | | |
| **Estimate Type (check all that apply – see BOE Report for estimate type by activity):**<br><br>_X_ Work Complete<br>_X_ Existing Purchase Order<br>_X_ Catalog Listing or Industrial Construction Database<br>_x_ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications<br>_x_ Engineering Estimate based on Similar Items or Procedures<br>_X_ Engineering Estimate based on Analysis<br>_x_ Expert Opinion | | |
| **Supporting Documents (including but not limited to):** | | |

## Details of the Base Estimate (explanation of the work)

This BoE covers the cost of development and construction of an ASIC ADC for the LTDB.

The labor estimate is obtained as follows:

- There remain three main steps: the nevis13 test chip, a 4-channel chip with full functionality (submitted for fabrication in February 2014), the prototype, expected to have a small number of improvements w.r.t. nevis13 (finalizing clock scheme, removal of any remaining test in- or outputs, etc.), and the final production chip.
- For the nevis13 and prototype chips the work is very similar: chip design and layout effort (EE and EE student); design and layout of three types of test boards: socketed board for functionality tests, precision board to measure full analog precision, and radiation board to measure SEE sensitivity (mainly EE); test board fabrication and assembly (ET); development of firmware and software for the test boards (EE, Instr. Physicist and uncosted Physicist); testing and documentation of test results (EE, ET, Instr. Physicist and uncosted Physicist). The estimates for these tasks are all based on our experience with the previous test chips and expectations for the evolution between the chips. More information on the expected evolution is given in the comments section below.
- The evolution between the prototype and final production chip is expected to be minimal (EE). After final submission and packaging preparation work, the main task will be to design, fabricate and set up the QA

infrastructure to efficiently test O(10k) chips (EE, ET, Instr. Physicist, Physicist). We expect that QA will be semi-automated: chips will be put in a socket and removed manually, but the measurement and logging of each chip's performance will be automatized. (See the comments section or QA sheet for a more detailed description of the planned QA procedure.) Including handling, testing, checking of the test results, inventory management and generation of documentation we expect this to take O(8 mins/chip). We estimate that approximately 20% of the chips will require triple this time because the chip requires more investigation, a malfunction of the test setup, or a problem in logging the test results. Testing itself will be done by ET's while investigation of problems will require Instr. Physicist time.

- For production of test boards we have typically allocated one week's worth of ET time. This includes getting quotes from the PCB manufacturer and assembler, relaying information between them and the engineers as needed, placing and tracking the requisitions, acquiring all the necessary parts, etc.

M&S costs are estimated as follows:

- The nevis13 chip and the prototype are expected to have a size slightly below 4x4 $mm^2$ leading to a cost estimate of $40k for fabrication (via CERN/MOSIS); nevis12 at 2x4$mm^2$ cost approx. $20k.
- The costs for the test boards is based on the actual cost of the test boards made for the nevis12 chip, as documented in the excel sheet included at the end of this document. Since many of the parts are common to the boards the total cost was approximately evenly split between the three types of boards.
- We have budgeted $30k in equipment costs for nevis13 precision testing. As we were testing the nevis12 chip we determined we needed a few items that we borrowed from the electrical engineering department, but had to return. These include a high precision signal generator with high output power (a candidate is the Agilent E4428C-UNB 503with high output power option – see quote), and a high precision multimeter (see quote).
- Irradiation costs correspond to (223 MeV proton) beam time at Massachusetts General Hospital (MGH), which is billed hourly. For nevis12 SEE testing, the beam cost was $3500 and travel cost $630.
- Production costs are estimated based on the contractual cost of mask and wafers (from the CERN contract, see the email message included at the end of the document), the 4x4$mm^2$ size estimate and a 70% production yield. One 8-in wafer then yields 1875 x 0.7 = 1300 chips. The US share of the production cost is 30%.
- Packaging: the cost estimate for production packaging is based on the attached quote from Quik Pak. The US share of the packaging cost is 30%.
- The QA board is expected to have a cost similar to the socketed test boards.
- For the QA test stand we will need to duplicate a substantial fraction of our development test stand as we need to keep the latter available for studies of failing chips and other measurements. The QA test stand does not require full precision equipment however, so should come in at reduced cost. (It will require a spectrum analyzer however.)
- Licenses: each year we pay $4000 for cadence (chip design) and $1500 for mentor graphics (board design) tools. These costs are included at the first occurrence of manufacturing of an item using these tools each FY.

Travel costs include irradiations (at MGH in Boston), trips to reviews at CERN for engineers and trips to BNL for integration assistance. Individual trip costs are based on past trips.

| Row Labels | Labor Hrs | Labor $ | M&S $ | Travel $ | Grand Total $ |
|---|---|---|---|---|---|
| 1.01.03.02.01 ASIC ADC for LTDB | 17,733 | 1,220,617 | 331,228 | 13,816 | 1,565,661 |
| 1.1.3.2.1.1 Nevis13 chip | 3,433 | 147,799 | 41,910 | 3,150 | 192,859 |
| Engineer | 344 | 43,871 | | | 43,871 |
| Inst-Phy | 828 | 65,015 | | | 65,015 |
| Technician | 508 | 29,220 | | | 29,220 |
| Student | 320 | 9,693 | | | 9,693 |
| Travel | | | | 3,150 | 3,150 |
| U-Postdoc | 619 | | | | 0 |
| U-Stu | 814 | | | | 0 |
| M&S | | | 41,910 | | 41,910 |
| 1.1.3.2.1.2 ADC Prototype | 6,484 | 426,563 | 75,130 | 5,850 | 507,543 |
| Engineer | 2,444 | 288,052 | | | 288,052 |
| Inst-Phy | 720 | 58,234 | | | 58,234 |
| Technician | 584 | 34,602 | | | 34,602 |
| Student | 1,476 | 45,675 | | | 45,675 |
| Travel | | | | 5,850 | 5,850 |
| U-Postdoc | 680 | | | | 0 |
| U-Stu | 580 | | | | 0 |
| M&S | | | 75,130 | | 75,130 |
| 1.1.3.2.1.3 ADC Production | 7,816 | 646,255 | 214,188 | 4,816 | 865,259 |
| Engineer | 3,432 | 399,292 | | | 399,292 |
| Inst-Phy | 1,400 | 118,008 | | | 118,008 |
| Technician | 2,000 | 123,189 | | | 123,189 |
| Student | 184 | 5,766 | | | 5,766 |
| Travel | | | | 4,816 | 4,816 |
| U-Postdoc | 400 | | | | 0 |
| U-Stu | 400 | | | | 0 |
| M&S | | | 214,188 | | 214,188 |

For actual costs incurred before May 1, 2014, please see the cost books.

## Assumptions:

Engineering will be available (i.e. no layoffs) and technology will remain available (as guaranteed by the contract between CERN and IBM).

## Risk Analysis

Schedule Risk: probability: moderate, impact: low; overall: low.

Potential problems: testing takes longer due to difficulties with complex test boards (probability moderate); the prototype is non-functional

Mitigation: extended testing time or additional prototyping round.

Cost Risk: probability: moderate, impact: moderate; overall: moderate.

Potential problems: technical problems require an extra round of prototyping; yields are lower than expected.

Mitigation: pay for an extra prototype round; buy more wafers.

Technical/Scope Risk: probability: low, impact: moderate; overall: low

Potential problem: prototype does not meet spec

Mitigation: extra round of prototyping

## M&S Contingency 19%

Contingency is determined on an activity-by-activity level guided by the contingency rule numbers, and rolled up to deliverable level. For activity-by-activity contingency numbers, please see the bottom-up risk and contingency spreadsheet.

## Labor Contingency 30%

## Comments:

This ADC has to satisfy stringent requirements: fast (40 MSPS), low power (150 mW/channel or less), low latency (as low as possible), radiation tolerant for HL-LHC, serialized outputs, low SEU rate. Nevis Labs has worked on the development of such a device using IBM CMOS 8RF technology, the CERN choice for the LHC upgrades. Test chips have established the validity of the design and have made it possible to estimate the amount of effort required for development of the prototype and production version, as well as testing infrastructure, testing and QA.

The ADC development work has been on track for approximately 6 years and has focused on eliminating technical risk. Over that period three test chips have been designed: the nevis09 chip contained an amplifier design which is at the core of the ADC's pipeline stages, and crucial to the ADC accuracy. This chip allowed us to develop the core of the design, but also learn about the technology, acquire experience with testing of high precision analog devices, and verify the radiation tolerance of IBM8RF for analog designs. The nevis10 chip contained two ADC channels each with four 1.5 bits/stage ADCs, designed to resolve the four most significant bits. The 1.5 bits, i.e. three possible codes to resolve one bit, furnish the redundancy needed for the application of a digital error correction. The analog residue was sent to a commercial ADC. Extensive testing and side-by-side comparison with a commercial 12-bit ADC showed that the analog performance of the nevis10 chip was at least as good as the commercial device's. Furthermore, irradiation up to 2 MRad showed no noticeable degradation in performance. The nevis12 chip, implementing two channels of 12-bit ADC (with four pipeline stages followed by an 8-bit successive approximation ADC block) with all supporting blocks (V and I reference, digital error correction, output serialization) was submitted for fabrication in November 2012 and testing is nearing completion. nevis12 has 11-bit performance at ~40 mW/channel and with ~80 ns latency, far better than the specifications. The lower analog performance, as well as infrequent generation of bad codes, has been traced to too large impedance in the reference voltage circuit, and insufficient clock duty cycle. Both issues have been addressed in the nevis13 chip through the redesign of the reference voltage circuit and the addition of a PLL whose design is inspired by the GBT PLL. Two series of SEE tests were run with the analysis being finalized. The final step is to understand the impact of chip heating during irradiation on analog performance.

The nevis13 chip was finalized in late 2013 and submitted along with the muon system VMM2 chip in February 2014. Testing is expected to start in the second half of May. Only small changes, based on test results, are expected between the nevis13 chip and the prototype. Test in- and outputs will be (almost) all be removed. These

adjustments will require revising the layout and another round of simulation. Changes between the prototype and the production chip are expected to be minimal, if any.

Production: we need O(10k) chips for the system. With 4x4mm$^2$ size and 70% yield we will get ~1300 good chips per wafer, i.e. we will need ~8 wafers. As the Non-recurring engineering (NRE) cost dwarfs the wafer cost we plan to be conservative and make sure we produce enough wafers. We plan for a production cost of $405k (NRE) + 8x $3.6k = $433.8k. The US share is 30%, approximately $130k. We estimate the packaging cost at $10/chip, so $100k with again a 30% US share. (We recently received a quote at $6/chip included below, although the packager indicated costs two years in the future are highly uncertain.)

QA: Every chip will be tested and characterized using a socketed board very similar to those used for functionality testing of the nevis12 and nevis13 chips. Our experience shows that the socket allows testing to 11 ENOB precision. Each chip will be inserted in the socket, the calibration constants will be calculated and FFTs will be acquired for three different carrier frequencies. All the data will be examined then logged in a database, and the chip will be removed and placed in the tray. We expect that for most chips (80%) the testing will take a few minutes, and to take into account handling, testing, checking of the test results, inventory management and generation of documentation we estimate an average of 8 mins/chip. We estimate that 20% of the chips will require more time because of problems with either the chip, the test stand, or the data storage. We estimate that on average such chips will take three times as long to characterize.

Details for tasks > 400 hours:

1.01.03.02.01 TDB2060 PC software (C# or C++) development - Balance
Instr. physicist 228 hrs, postdoc 95 hrs, student 190 hrs
This is for the development of the software associated with testing, including device drivers, control functions and analysis. The estimate is based on experience with testing the nevis09, nevis10 and nevis12 chips.

1.01.03.02.01 TDB2120 Test Preparation
ET 180 hrs, EE student 400 hrs, instr. physicist 250 hrs, Sr. EE 320 hrs, postdoc 180 hrs, student 180 hrs
1.01.03.02.01 TDB2125 Testing
ET 220 hrs, instr. physicist 240 hrs, postdoc 300 hrs, student 400 hrs
These two activities are the main testing of the nevis13 chip. Test preparation involves work on test boards (preparation, debugging, implementing fixes), whereas the testing itself includes running the tests, understanding the results, devising further tests to that end, etc. The estimate is based on our experience with the nevis10 and nevis12 test chips.

1.01.03.02.01 TDB2180 Redesign Nevis13 blocks as needed for prototype
EES 632 hrs, Jr. EE 488 hrs, Sr. EE 632 hrs
This includes making any changes we deem necessary between the nevis13 chip and the prototype, performing corresponding simulations, both pre- and post-layout, and finalizing the files for tapeout. Our expectation is that the changes will be rather small, so this is substantially less than the effort spent on the nevis10 or nevis12 chips.

1.01.03.02.01 TDB2210 Test board firmware development
EES 40 hrs, instr. physicist 200 hrs, Jr. EE 160 hrs, Sr. EE 80 hrs

This is the development of firmware for the prototype testboard. This is based on experience with the nevis10 and nevis12 testboards, somewhat reduced as we expect few new features. (E.g. nevis12 introduced I2C.)

1.01.03.02.01 TDB2220 Precision Test board PCBs (Schematic and layout)
EES 180 hrs, Jr. EE 304 hrs, Sr. EE 240 hrs
This is based on experience with the nevis10 and nevis12 testboards. It is likely that we will go to a higher end FPGA to increase our DAQ bandwidth.

1.01.03.02.01 TDB2240 PC software (C# or C++) development
Instr. physicist 240 hrs, postdoc 100 hrs, student 100 hrs
This is for the development of the software associated with testing, including device drivers, control functions and analysis. The estimate is based on experience with testing the nevis09, nevis10 and nevis12 chips.

1.01.03.02.01 TDB2310 Precision Testing
ET 400 hrs, EE student 464 hrs, instr. physicist 200 hrs, Jr. EE 120 hrs, Sr. EE 300 hrs, postdoc 500 hrs, student 400 hrs
This involves work on test boards (preparation, debugging, implementing fixes), running the tests, understanding the results, devising further tests to that end, etc. The estimate is based on our experience with the nevis10 and nevis12 test chips.

1.01.03.02.01 TDB2340 Radiation test preparation (setup, software)
EE student 160 hrs, instr. physicist 80 hrs, Jr. EE 40 hrs, postdoc 80 hrs, student 80 hrs
The radiation test is quite specific in the required monitoring and tests, so this is dedicated to ensuring the plan is well-defined and everything is ready to maximize the returns. The estimate is based on previous tests.

1.01.03.02.01 TDB2380 Final chip submission preparation
EES 184 hrs, Jr. EE 280 hrs, Sr. EE 200 hrs
This is to re-check all the files and prepare the layout on the reticle. The estimate is based on experience in submitting the nevis12 and nevis13 chips.

1.01.03.02.01 TDB2440 QA board software
Instr. physicist 200 hrs, postdoc 200 hrs, student 200 hrs
This is to develop the QA board software, where everything needs to be automatized. The estimate is based on software development work for the test chips.

1.01.03.02.01 TDB2470 QA test stand setup
ET 80 hrs, instr. physicist 200 hrs, Jr. EE 200 hrs, postdoc 200 hrs, student 200 hrs
This is to set up the QA test stand, incl. hardware, environment, storage of results, etc. The estimate is based on testing work, as well as QA work done for initial ATLAS construction.

1.01.03.02.01 TDB2482 Chip test--part 1
ET 920 hrs, instr. physicist 200 hrs

1.01.03.02.01 TDB2492 Chip test-part 2
ET 920 hrs, instr. physicist 200 hrs
These estimates are detailed in the QA sheets.

1.01.03.02.01 TDB2510 Integration support
instr. physicist 400 hrs, Jr. EE 1064 hrs, Sr. EE 848 hrs
This involves assisting in debugging/understanding the pre-production LTDB behavior, and writing detailed documentation ("Data sheet"). This estimate is based on experience with ATLAS FEB and D0 L1Calo debugging and production.

Summary of M&S costs (quotes are included below):

| 1.1.3.2.1 M&S costs | | | |
|---|---|---|---|
| | | | |
| Activity ID | Description | Unburdened | |
| TDB2070 | Nevis13 precision board PCB | $2,000 | |
| TDB2090 | Nevis13 packaging | $1,500 | TDB2050, 2070, 2090, 2100, 2140: $20,500 for boards |
| TDB2100 | Nevis13 precision board assembly | $5,000 | (see nevis12 test board costs) + $1500 mentor license |
| TDB2120 | Precision testing | $24,000 | Signal generator/measurement equipment |
| TDB2140 | Nevis13 Rad board prod and assembly | $5,000 | TDB2050, 2070, 2090, 2100, 2140: $20,500 for boards (see nevis12 test board costs) + $1500 mentor license |
| TDB2160 | Radiation tests | $3,500 | Beam billed by the hour, from nevis12 tests |
| | | | |
| TDB2200 | Prototype submission | $44,000 | $40k silicon + $4000 cadence license |
| TDB2230 | Socketed board prod and assembly | $8,500 | |
| TDB2250 | Precision board PCB | $2,000 | |
| TDB2270 | Prototype packaging | $1,500 | |
| TDB2290 | Precision board assembly | $5,000 | $20,500 for boards (see nevis12 test board costs) + |
| TDB2330 | Rad board prod and assembly | $5,000 | $1500 mentor license |
| TDB2340 | Rad test preparation | $2,000 | Cables etc. (educated guess) |
| TDB2350 | Rad testing | $3,500 | Beam billed by the hour, from nevis12 tests |
| | | | |
| TDB2410 | Production | $130,000 | 30% (US share) of $405k (NRE) + 8x$3600 (wafers) |
| TDB2450 | QA Board prod and assembly | $8,500 | $7000 (as for TDB2230) + $1500 mentor license |
| TDB2460 | Packaging | $30,000 | 30% (US share) of $100,000 ($10/chip x 10k chips) |
| TDB2470 | QA test stand | $25,000 | Duplicate development test stand |
| TDB2485 | Radiation tests | $3,500 | Beam billed by the hour, from nevis12 tests |

Nevis12 chip packaging and test board costs. The total is $20,897 for three types of test boards (socketed, precision and radiation).

| MANUFACTURER | PART NUMBER | ITEM | VENDOR | DATE | DEL | ORDERED | COST @ | COST | REC'D | DATE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| ON SEMICONDUCTOR | NB6L14SMNG | 1 | DIGI KEY | 9/5/12 | STOCK | 10 | $5.63 | $56.25 | 10 | 9/17/12 |
| ON SEMICONDUCTOR | NB6L14SMNG | 1 | DIGI KEY | 9/5/12 | STOCK | 10 | $5.63 | $56.25 | 10 | 9/18/12 |
| PLASTRONICS SOCKET COMPANY | 72QN50HS1100100 | 1 | PLASTRONICS SOCKET COMPANY | 1/22/13 | 2-3 WEEKS A | 2 | $187.70 | $375.40 | 2 | 2/12/13 |
| QUIK-PAK | QP-QFN72-10mm-0.5MM | 1 | QUIK=PAK | 1/22/13 | 3 DAYS | 30 | $9.26 | $277.80 | 30 | 3/6/13 |
| QUIK-PAK | REMOLDED TO 0.8MM HEIGHT: HAND MARKED | 2 | QUIK=PAK | 1/22/13 | 3 DAYS | 1 | $1,122.00 | $1,122.00 | 1 | 3/6/13 |
| TEXAS INSTRUMENTS | CDCP1803MRGETEP | 1 | TEXAS INSTRUMENTS | 1/22/13 | ASAP | 3 | $0.00 | $0.00 | 3 | 1/28/13 |
| ELECTROTEK | Nevis12_Tester & Nevis12_Checker Rev. 1.0 | 1 | ELECTROTEK | 1/24/13 | 10 DAYS | 28 | $66.36 | $1,858.08 | 28 | 2/13/13 |
| ELECTROTEK | Nevis12_Tester & Nevis12_Checker Rev. 1.0 | 1 | ELECTROTEK | 1/24/13 | 10 DAYS | 1 | $600.00 | $600.00 | 1 | 2/13/13 |
| ELECTROTEK | Nevis12_Tester & Nevis12_Checker Rev. 1.0 | 2 | ELECTROTEK | 1/24/13 | 10 DAYS | 1 | $250.00 | $250.00 | 1 | 2/13/13 |
| ANALOG DEVICES | AD8031ARTZ-R2 | 1 | ARROW | 1/29/13 | STOCK | 25 | $3.13 | $78.25 | 25 | 2/7/13 |
| ALTERA | EP3C5F256C6N | 2 | ARROW | 1/29/13 | STOCK | 10 | $26.80 | $268.00 | 10 | 2/7/13 |
| MURATA | LQH2MCN100K02L | 3 | ARROW | 1/29/13 | STOCK | 3000 | $0.08 | $252.00 | 3000 | 2/7/13 |
| PANASONIC | ERJ-2RKF6980X | 4 | ARROW | 1/29/13 | STOCK | 10000 | $0.00 | $27.00 | 10000 | 2/7/13 |
| PANASONIC | ERJ-2RKF49R9X | 5 | ARROW | 1/29/13 | STOCK | 10000 | $0.00 | $27.00 | 10000 | 2/7/13 |
| PANASONIC | ERJ-2RKF1500X | 6 | ARROW | 1/29/13 | STOCK | 10000 | $0.00 | $27.00 | 10000 | 2/7/13 |
| PANASONIC | ERJ-3EKF4702X | 7 | ARROW | 1/29/13 | STOCK | 5000 | $0.00 | $8.00 | 5000 | 2/7/13 |
| PANASONIC | ERJ-3EKF1200X | 8 | ARROW | 1/29/13 | STOCK | 5000 | $0.00 | $8.00 | 5000 | 2/7/13 |
| MURATA | GRM31CR61E106KA12L | 9 | ARROW | 1/29/13 | STOCK | 2000 | $0.05 | $104.00 | 2000 | 2/7/13 |
| MURATA | PVG5A503C01R00 | 1 | MOUSER | 1/30/13 | STOCK | 250 | $2.69 | $672.50 | 250 | 2/7/13 |
| TEXAS INSTRUMENTS | CDCP1803MRGETEP | 1 | DIGI KEY | 1/30/13 | STOCK | 25 | $12.03 | $300.83 | 25 | 2/11/13 |
| TDK | C1608X5RR1C475K080AC | 2 | DIGI KEY | 1/30/13 | STOCK | 4000 | $0.06 | $222.00 | 4000 | 2/11/13 |
| PANASONIC | ERA-6AEB102V | 3 | DIGI KEY | 1/30/13 | STOCK | 1000 | $0.08 | $76.95 | 1000 | 2/11/13 |
| MINI CIRCUITS | ADT1-6T+ | 1 | MINI CIRCUITS | 1/31/13 | 1 WK | 50 | $3.40 | $170.00 | 50 | 2/5/13 |
| CTS FREQUENCY CONTROLS | ATS060-8 | 1 | DIGI KEY | 2/1/13 | STOCK | 100 | $0.23 | $23.20 | 100 | 2/11/13 |
| SUSUMU | RG2012P-111-B-T5 | 2 | DIGI KEY | 2/1/13 | STOCK | 1000 | $0.10 | $103.42 | 1000 | 2/11/13 |
| TYCO/AMP | 2-1614884-8 | 3 | DIGI KEY | 2/1/13 | STOCK | 1000 | $0.15 | $147.32 | 1000 | 2/11/13 |
| PANASONIC | ERA-6AEB64R9V | 4 | DIGI KEY | 2/1/13 | STOCK | 5000 | $0.04 | $213.75 | 5000 | 2/11/13 |
| PANASONIC | ERJ-2RKF1003X | 5 | DIGI KEY | 2/1/13 | STOCK | 10000 | $0.00 | $34.70 | 10000 | 2/11/13 |
| APPLICAD INC | NEVIS12_CHECKER | 1 | APPLICAD INC | 2/1/13 | 10 DAYS | 2 | $560.00 | $1,120.00 | 2 | 3/6/13 |
| APPLICAD INC | NEVIS12_CHECKER | 1 | APPLICAD INC | 2/1/13 | 10 DAYS | 2 | $300.00 | $600.00 | 2 | 3/6/13 |
| APPLICAD INC | NEVIS12_CHECKER | 2 | APPLICAD INC | 2/1/13 | 10 DAYS | 1 | $500.00 | $500.00 | 1 | 3/6/13 |
| APPLICAD INC | NEVIS12_CHECKER | 3 | APPLICAD INC | 2/1/13 | 10 DAYS | 1 | $400.00 | $400.00 | 1 | 3/6/13 |
| SUSUMU | RG2012P-121-B-T5 | 1 | DIGI KEY | 2/4/13 | STOCK | 1000 | $0.10 | $103.42 | 1000 | 2/14/13 |
| MCMASTER CARR | 95475A115 | 1 | MCMASTER CARR | 3/15/13 | STOCK | 2 | $7.85 | $15.70 | 2 | 3/18/13 |
| MCMASTER CARR | 90631A003 | 2 | MCMASTER CARR | 3/15/13 | STOCK | 1 | $3.45 | $3.45 | 1 | 3/18/13 |
| SCHOVAERS | AnyLevel2LVDS | 1 | SCHOVAERS | 4/11/13 | 1 WK | 10 | $9.74 | $97.40 | 10 | 4/22/13 |
| SCHOVAERS | AnyLevel2LVDS | 2 | SCHOVAERS | 4/11/13 | 1 WK | 1 | $40.00 | $40.00 | 1 | 4/22/13 |
| ON SEMICONDUCTOR | MC100EPT20DG | 1 | ARROW | 4/26/13 | STOCK | 30 | $5.06 | $151.80 | 30 | 5/7/13 |
| SAMTEC | TSW-102-07-G-S | 2 | ARROW | 4/26/13 | STOCK | 500 | $0.06 | $29.30 | 500 | 5/14/13 |
| APPLICAD INC | NEVIS12_TESTER | 1 | APPLICAD INC | 5/9/13 | 3 WKS | 2 | $425.00 | $850.00 | 2 | 6/10/13 |
| APPLICAD INC | NEVIS12_TESTER | 2 | APPLICAD INC | 5/9/13 | 3 WKS | 2 | $300.00 | $600.00 | 2 | 6/10/13 |
| APPLICAD INC | NEVIS12_TESTER | 3 | APPLICAD INC | 5/9/13 | 3 WKS | 1 | $500.00 | $500.00 | 1 | 6/10/13 |
| APPLICAD INC | NEVIS12_TESTER | 4 | APPLICAD INC | 5/9/13 | 3 WKS | 1 | $400.00 | $400.00 | 1 | 6/10/13 |
| APPLICAD INC | NEVIS12_TESTER | 5 | APPLICAD INC | 5/9/13 | 3 WKS | 1 | $150.00 | $150.00 | 1 | 6/10/13 |
| ELECTROTEK | Nevis12_Radiation_Tester | 1 | ELECTROTEK | 6/14/13 | 10 DAYS | 6 | $323.13 | $1,938.78 | 6 | 7/1/13 |
| ELECTROTEK | Nevis12_Radiation_Tester | 1 | ELECTROTEK | 6/14/13 | 10 DAYS | 1 | $300.00 | $300.00 | 1 | 7/1/13 |
| ELECTROTEK | Nevis12_Radiation_Tester | 2 | ELECTROTEK | 6/14/13 | 10 DAYS | 1 | $250.00 | $250.00 | 1 | 7/1/13 |
| MINI CIRCUITS | ADT1-6T+ | 1 | MINI CIRCUITS | 6/19/13 | 1 WK | 100 | $3.35 | $335.00 | 100 | 6/21/13 |
| FTDI | FT2232D | 1 | DIGI KEY | 6/24/13 | STOCK | 10 | $6.28 | $62.80 | 10 | 7/1/13 |
| LINEAR TECHNOLOGY | LTC3026EMSE#PBF | 2 | DIGI KEY | 6/24/13 | STOCK | 60 | $3.14 | $188.40 | 60 | 7/1/13 |
| MURATA | PVG5A202C01R00 | 3 | DIGI KEY | 6/24/13 | STOCK | 250 | $2.02 | $505.31 | 250 | 7/1/13 |
| AMPHENOL | 132136 | 1 | MOUSER | 6/24/13 | STOCK | 100 | 4.23 | $423.00 | 100 | 6/27/13 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| ALTERA | EP3C5F256C6N | 2 | MOUSER | 6/24/13 | STOCK | 12 | 26.26 | $315.12 | 12 | 6/27/13 |
| ANALOG DEVICES | AD8031ARTZ-R2 | 3 | MOUSER | 6/24/13 | STOCK | 20 | 2.35 | $47.00 | 20 | 6/27/13 |
| AMP / TYCO | 292304-1 | 1 | ARROW | 6/24/13 | STOCK | 10 | $0.61 | $6.14 | 10 | 6/28/13 |
| SAMTEC | TSW-105-07-G-D | 2 | ARROW | 6/24/13 | STOCK | 100 | $0.29 | $29.00 | 100 | 6/28/13 |
| MICREL | MIC39100-2.5WS | 3 | ARROW | 6/24/13 | STOCK | 75 | $0.71 | $52.95 | 75 | 6/28/13 |
| MICREL | MIC39100-3.3WS | 4 | ARROW | 6/24/13 | STOCK | 50 | $0.75 | $37.40 | 50 | 6/28/13 |
| ON SEMICONDUCTOR | NB6L14SMNG | 5 | ARROW | 6/24/13 | STOCK | 75 | $2.96 | $222.00 | 75 | 6/28/13 |
| PANASONIC | ERA-6AEB203V | 6 | ARROW | 6/24/13 | STOCK | 5000 | $0.04 | $180.00 | 5000 | 6/28/13 |
| PANASONIC | ERJ-6ENF7501V | 7 | ARROW | 6/24/13 | STOCK | 5000 | $0.00 | $16.00 | 5000 | 6/28/13 |
| PANASONIC | ERJ-6EKF4022V | 8 | ARROW | 6/24/13 | STOCK | 5000 | $0.00 | $8.00 | 5000 | 6/28/13 |
| APPLICAD INC | NEVIS12_RADIAITION_TESTER | 1 | APPLICAD INC | 6/24/13 | 3 WKS | 5 | $290.00 | $1,450.00 | 5 | 7/19/13 |
| APPLICAD INC | NEVIS12_RADIAITION_TESTER | 1 | APPLICAD INC | 6/24/13 | 3 WKS | 2 | $300.00 | $600.00 | 2 | 7/19/13 |
| APPLICAD INC | NEVIS12_RADIAITION_TESTER | 2 | APPLICAD INC | 6/24/13 | 3 WKS | 1 | $400.00 | $400.00 | 1 | 7/19/13 |
| APPLICAD INC | NEVIS12_RADIAITION_TESTER | 3 | APPLICAD INC | 6/24/13 | 3 WKS | 1 | $400.00 | $400.00 | 1 | 7/19/13 |
| PTC | | 1 | AMAZON.COM | 8/22/13 | STOCK | 1 | $33.39 | $33.39 | 1 | 8/28/13 |
| POMONA | 4288 | 1 | HEILIND ELECTRONICS | 8/26/13 | 2 WKS | 5 | $12.20 | $61.00 | 5 | 9/18/13 |
| AMPHENOL | 031-219-RFX | 2 | HEILIND ELECTRONICS | 8/26/13 | 2 WKS | 25 | $2.85 | $71.25 | 25 | 9/11/13 |
| MOLEX | 460123242 | 1 | MOLEX | 8/26/13 | ASAP | 50 | $0.00 | $0.00 | 50 | 8/28/13 |
| MOLEX | 460123242 | 1 | MOLEX | 8/26/13 | ASAP | 100 | $0.43 | $43.40 | 100 | 8/30/13 |

Production cost in IBM CMOS 8RF. We expect we will need 8 wafers.

The tax is included.

Cheers, Philippe


Philippe Farthouat Tel: +41 (0)22 767 6221
PH Department Mobile: +41 (0)76 487 5318
CERN Fax: +41 (0)22 766 9576
CH-1211 Geneva 23 Email: Philippe.Farthouat@cern.ch
Switzerland


Le 6 oct. 2011 à 23:12, Gustaaf Brooijmans a écrit :

> Hi,
>
> Yes, those are the numbers I had. Just for completeness, does this include the 7% cern "tax" (for the use of the mixed signal kit)?
>
> Thx
>
> Gustaaf
>
> On 10/6/11 5:05 PM, Philippe Farthouat wrote:
>> Dear Francesco,
>>
>> The cost for the 130 nm is as follows:
>> - an engineering run costs 405 kUSD (I think with all options) and it covers the NRE and 2 wafers
>> - each additional wafer costs 3.6 kUSD
>>
>> Cheers, Philippe
>>
>> 
>> Philippe Farthouat Tel: +41 (0)22 767 6221
>> PH Department Mobile: +41 (0)76 487 5318
>> CERN Fax: +41 (0)22 766 9576
>> CH-1211 Geneva 23 Email: Philippe.Farthouat@cern.ch
>> Switzerland
>> 

New signal generator (E4428C 503) and UNB option:

TESTEQUITY

| QUOTATION | | |
|---|---|---|
| **Quotation No.** 298382 | **Quotation Date** May 02, 2014 | **Page Number** 1 of 1 |
| **Revision No.** 1 | **Customer Number** 875464 | |

**Customer Address:**
Columbia University-Nevis
136 South Broadway
Irvington, NY 10533

**Attention:** Nancy Bishop
**Telephone No:** 914-591-2855
**E-Mail:** bishop@nevis.columbia.edu

**TestEquity Sales Office**
TestEquity LLC
6100 Condor Drive
Moorpark, CA
93021 United States
**Fax No:** 800-272-4329 / 805-498-3733
**Web:** http://www.testequity.com

**For assistance, please contact us:**

**Jim Blue - Sr. Account Executive**
**Telephone No:** 800-732-3457 / 805-498-9933 x123
**E-Mail:** Jim.Blue@TestEquity.com

**Your local Account Manager is:**

**Brian Saunders - Account Manager**
**Telephone No:** 1-800-732-3457 x 272
**Cell No:** 1-914-805-5641

**Please reference the TestEquity Quotation No. 298382.**

| Item | Type | Mfr | Model and Description | Qty | Mfr List Price | Sale Price |
|---|---|---|---|---|---|---|
| 1 | *N | **Agilent** | **E4428C**<br>ESG analog signal generator<br>Lead Time: Estimated ship date 4 Weeks ARO | 1 | 0.00 | **0.00** |
| 2 | *N | **Agilent** | **E4428C-UNB**<br>High output power with mechanical attenuator<br>Lead Time: Estimated Ship Date 4 Weeks ARO | 1 | 1,847.00 | **1,477.60** |
| 3 | *N | **Agilent** | **E4428C-503**<br>Frequency range from 250KHz to 3GHz<br>Lead Time: Estimated Ship Date 4 Weeks ARO | 1 | 27,739.00 | **22,191.20** |
| | | | | **Quote Net Total** | **$29,586.00** | **$23,668.80** |

**Financing Option**
Lease the above equipment for: $1,006 per month. Lease Term: 36 months w/ $1 buyout.
24, 48, and 60-month financing programs are also available.
Lease rates and terms may vary and a deposit may be required, and are subject to credit approval.

NOTES:

*N-New equipment comes with full manufacturer's warranty.

*Manufacturer's list prices are included for reference only, and are subject to change without notice.

*Prices are quoted in US dollars, FOB Moorpark, California, and do not include shipping costs, applicable taxes, tariffs or duties. Unless otherwise noted, quotations are valid for 30 days, subject to manufacturer price changes. Equipment availability is subject to prior sale or rental.

*Standard payment terms are N30 for all purchases and are subject to credit approval.

Packaging quote (the package is the one used for nevis13, and expected for the final chip). This yiels $6/chip, but we have been told the future cost is highly uncertain and have therefore used $10/chip.

Quik-Pak™
Microelectronic Packaging & Assembly Solutions

OPEN·molded Plastic Package℠

Quote#: 10752


*Quik-Pak*
*10987 Via Frontera*
*San Diego, CA 92127*
*Ph. - (858) 674-4676*
*Fax - (858) 674-4681*
bill@icproto.com


*Name: Nancy Bishop*
*Company: Columbia Univ. Nevis Labs*
*Location: NY*
*Date: 2/20/2014*

*Budgetary Quote (Conservative): 10,000 pieces*

| Qty | | Description | Unit Price | | Line Total |
|---|---|---|---|---|---|
| 10000 | | 72 Pin 10mmx10mm Air Cavity Assembled QFN | $6.00 | | $ 60,000.00 |
| | | Includes wafer finishing, air cavity package, lid, wire bonding, lid seal and branding | | | |
| | | *TBD TURN* | | | |
| | | | | | |
| Note: Pricing above may be revised if scope of work changes | | | | **Subtotal** | $ 60,000.00 |
| | | | | | |
| | | | | *Total* | $ 60,000.00 |

by: *Bill Lawrence*
***East Coast Sales Manager***

Digital multimeter:

TESTEQUITY

| QUOTATION | | |
|---|---|---|
| Quotation No. 293023 | Quotation Date March 17, 2014 | Page Number 1 of 3 |
| Revision No. 1 | Customer Number 875464 | |

**Customer Address:**
Columbia University-Nevis
136 South Broadway
Irvington, NY 10533

**Attention:** Nancy Bishop
**Telephone No:** 914-591-2855
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**Cell No:** 1-914-805-5641

**Please reference the TestEquity Quotation No. 293023.**

| Item | Type | Mfr | Model and Description | Qty | Mfr List Price | Sale Price |
|---|---|---|---|---|---|---|
| 1 | *N | **Agilent** | **34411A**<br>Digital multimeter/Digitizer, 6.5 digit<br>TE P/N 15944.1<br>Lead Time: In Stock | 1 | 2,235.00 | **1,788.00** |
| | | | | **Quote Net Total** | **$2,235.00** | **$1,788.00** |

NOTES:

*N-New equipment comes with full manufacturer's warranty.

*Manufacturer's list prices are included for reference only, and are subject to change without notice.

*Prices are quoted in US dollars, FOB Moorpark, California, and do not include shipping costs, applicable taxes, tariffs or duties. Unless otherwise noted, quotations are valid for 30 days, subject to manufacturer price changes. Equipment availability is subject to prior sale or rental.

*Standard payment terms are N30 for all purchases and are subject to credit approval.